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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,762	10/15/2003	Shiv Kumar Gupta	15164US01	6313

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EXAMINER	
GEBRESILASSIE, KIBROM K	
ART UNIT	**PAPER NUMBER**
2128	

MAIL DATE	DELIVERY MODE
07/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,762	GUPTA, SHIV KUMAR	
	Examiner	Art Unit	
	Kibrom K. Gebresilassie	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amended application filed on 04/16/2007.

2. Claims 1-5 are pending.

3. Claims 6-11 are canceled and therefore rejections are withdrawn.

Response to Arguments

4. Response to 101 rejection: Applicant's arguments filed 04/16/2007 have been fully considered but they are not persuasive.

a. Applicants argued:

The specification does not indicate that the claimed "first circuitry" and the claimed "second circuitry" are just software per se. Further, applicant indicated that examiner to look at paragraph [0023], which states as follows:

> "The hardware emulator 200 comprises a sea of logic and other circuitry 205. The sea of logic and other circuitry 205 is configurable to realize a vast number of integrated circuits. The sea of logic and other circuitry can be divided into a plurality of portions 210. One portion 210(1) can be configured to realize a first SOC, SOC1. The second portion 210(2) can be configured to realize a second SOC, SOC2."

In response, the paragraph shown above does not indicate or define whether the "first circuitry" or the "second circuitry" are physical components. Further, applicants have not explained how the above paragraph or anywhere in

the specification make the "first circuitry" and "second circuitry" somehow are physical components.

5. Response to 102(b) rejection: Applicant's arguments filed 04/16/2007 have been fully considered but they are not persuasive.

b. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

c. Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

d. Applicants argued:

> It is respectfully submitted that "emulator of Hardware Model B" and "emulator of Hardware Model C" do not teach "a hardware emulator ... further comprising: a first circuitry ... and a second circuitry". Accordingly, Examiner is requested to withdraw the rejection to claim 1 and dependent claims 2 and 3.
>
> Additionally, Examiner is requested to withdraw the rejection to claims 4

In response the prior art of reference discloses a plurality of hardware emulators (i.e. first and second circuitries) that verify multi-chip system, which is constructed from selected hardware model as shown in Fig. 1 #26 (**See: Col. 5 lines 3-16, lines 24-33; Fig. 1 #31, #23, #35, #37, #21).**

6. Examiner finds applicants argument unpersuasive and rejection is maintained.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1-4 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed inventions do not seem to require any hardware to perform their function. As such, the claims appear to be a system of software per se and are therefore non-statutory. A claim that recites a piece of software alone without any link to a hardware component is directed to non-statutory subject matter since there is no relationship between the computer software and hardware components which permits the functionality of the software to be realized.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by US. Patent No. 6,298,452 issued to Hill et al.

1. (Currently Amended)

Hill discloses a system for verifying a plurality of systems on a plurality of chips (**See: Col. 5 lines 56-57**), said system comprising:

a hardware emulator for verifying the plurality of systems on the plurality of chips (**See: Col. 24-26**), said hardware emulator further comprising:

a first circuitry for verifying a first system on a chip (**See: Col. 5 lines 24-33, lines 46-55**), said first circuitry further comprising at least one output for providing testing results from the first system on the chip (**See: Fig. 6 and corresponding texts**); and

a second circuitry for verifying a second system on another chip while verifying the first system on chip (**See: Abstract, Col. 5 lines 24-33**).

2. (Currently Amended)

Hill discloses the system of claim 1, wherein the hardware emulator further comprises:

a first interface for providing inputs to the first circuitry and receiving outputs from the first circuitry (**See: Fig. 1 #27 #29 and corresponding texts**); and

a second interface for providing inputs to the second circuitry and receiving outputs from the second circuitry (**See: Fig. 1 #27 #29 and corresponding texts**).

3. (Currently Amended)

Hill discloses the system of claim 1, wherein the first circuitry is configured to realize the first system on a chip and the second circuitry is configured to realize the second system on another chip (**See: Col. 5 lines 25-26**).

4. (Currently Amended)

Hill discloses a system for verifying a plurality of systems on a plurality of chips (**See: Col. 1 lines 3-6**), said system comprising:

a hardware emulator (**See: Fig. 1 #31 #23 and corresponding texts**) comprising:

a first circuitry configured to realize a first system on a chip (**See: Col. 5 lines 24-33, lines 46-55**), said first circuitry further comprising at least one output for providing testing results from the first system on the chip (**See: Fig. 6 and corresponding texts**); and

a second circuitry configured to realize a second system on another chip while verifying the first system on chip, the second circuitry connected to the first circuitry (**See: Abstract, Col. 5 lines 24-33**).

5. (Original)

Hill discloses the system of claim 4, wherein the hardware emulator further comprises:

a first interface operably connected to the first circuitry, wherein the first interface provides inputs to the first circuitry and receives outputs from the first circuitry (**See: Fig. 1 #27 #29 and corresponding texts**); and

a second interface operably connected to the second circuitry, wherein the second interface provides inputs to the second circuitry and receives outputs from the second circuitry (**See: Fig. 1 #27 #29 and corresponding texts**).

6-11. (Cancelled).

Conclusion

9. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is

571-272-8571. The examiner can normally be reached on 8:00 am - 4:30 pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KG

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